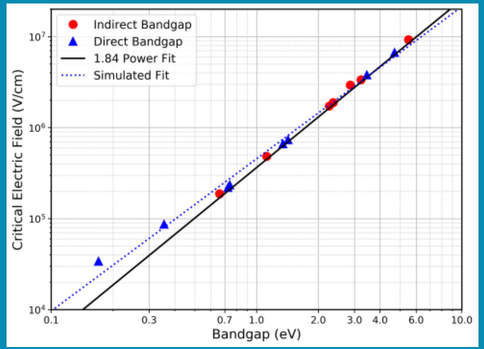
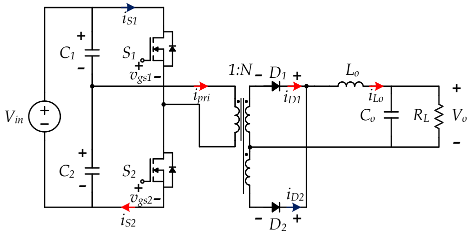


Reliability Studies of Wide-Bandgap Power Semiconductor Devices Under Realistic Stress Conditions



R. Kaplar, J. Flicker, O. Slobodyan, J. Mueller, L. Garcia Rodriguez, A. Binder, J. Dickerson, T. Smith, and S. Atcitty

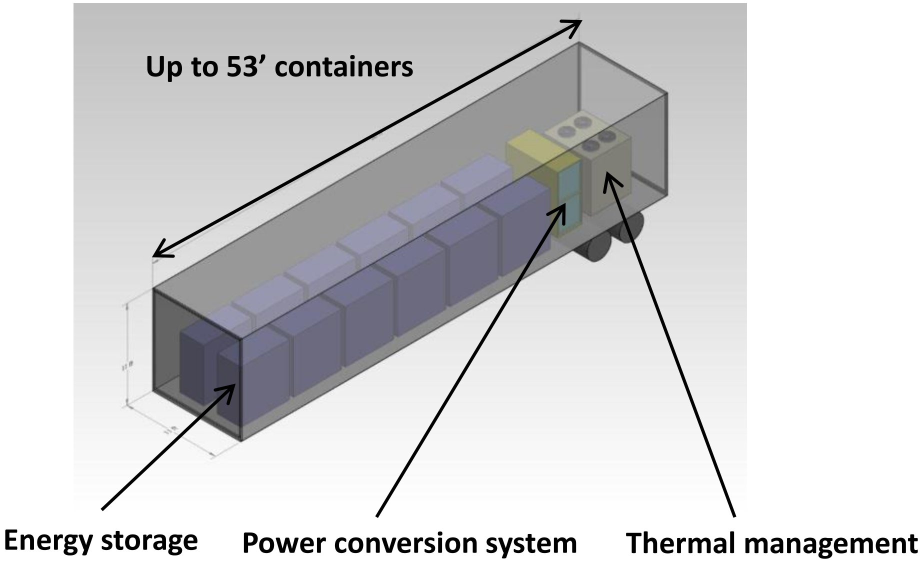
Sandia National Laboratories, Albuquerque NM

DOE Office of Electricity – Energy Storage Program
Virtual Peer Review – September 29, 2020

Acknowledgement

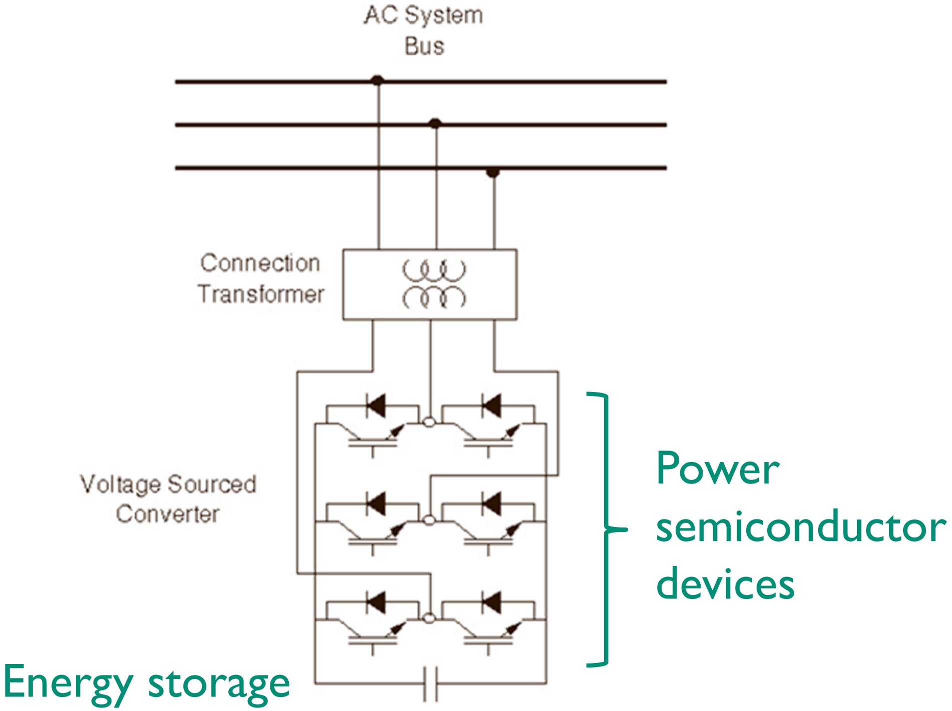
We thank the DOE Office of Electricity Energy Storage Program managed by Dr. Imre Gyuk for supporting the work at Sandia National Laboratories

WBG Power Electronics for Energy Storage



Typical Applications

- Grid stabilization
- Frequency regulation
- Renewable integration
- Peak shaving
- Voltage support



Benefits of portable storage

- Low installation cost
- Short time from installation to operation
- System is optimized for use at multiple sites

Typical portable power conversion system

- PWM voltage sourced converter
- Silicon-based power electronics
- Water cooled (*complex, bulky, and expensive*)

Project Motivation and Goals

- **Power electronic systems are a necessary interface between energy storage systems and the electric grid**
- **Wide-bandgap semiconductors have material properties that make them theoretically superior to silicon for power conversion applications**
  - Higher switching frequencies plus lower conduction and switching losses reduce the size and complexity of power conversion systems, **thus reducing the overall system cost**
  - However, questions remain regarding the performance and reliability of wide-bandgap materials and devices, **limiting their implementation**

Program goal: Understand performance and reliability of wide-bandgap power switches & how this impacts circuit- and system-level performance and cost

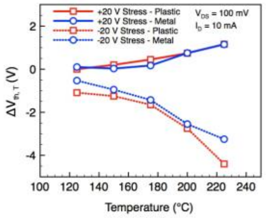
Program Historical Highlights

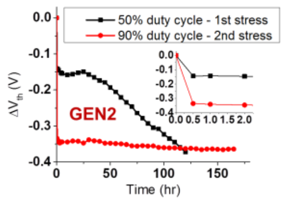
2009

Suggested reliability improvements for components, software, and operation of Silicon Power Corporation's Solid-State Current Limiter

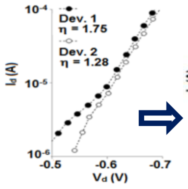
Developed and documented a general process for analyzing the reliability of any power electronics system

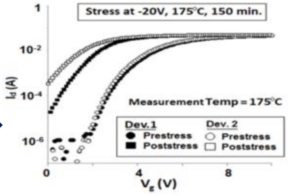
Characterized and evaluated commercial SiC MOSFETs, including the impacts of bias, temperature, packaging, and AC gate stress on reliability



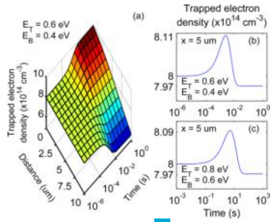


Developed models for SiC threshold voltage instability, and identified the free-wheeling diode ideality factor as a potential screening metric for threshold voltage shifts

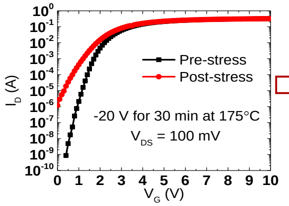


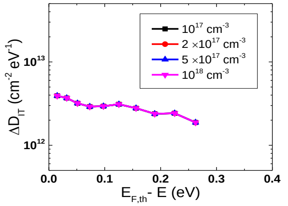


Created a physics-based model for GaN HEMTs linking defect properties to device design



Developed an easy to use method that can be used by circuit designers to evaluate the reliability of commercial SiC MOSFETs



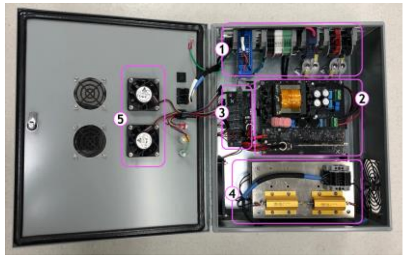


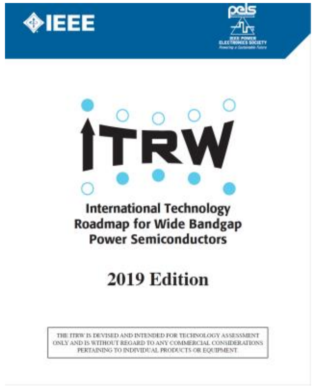
Characterized switching of vertical GaN PiN diodes using double-pulse test circuit

JEDEC

Participating in JEDEC WBG reliability working group

Constructed half-bridge hard-switching test circuit



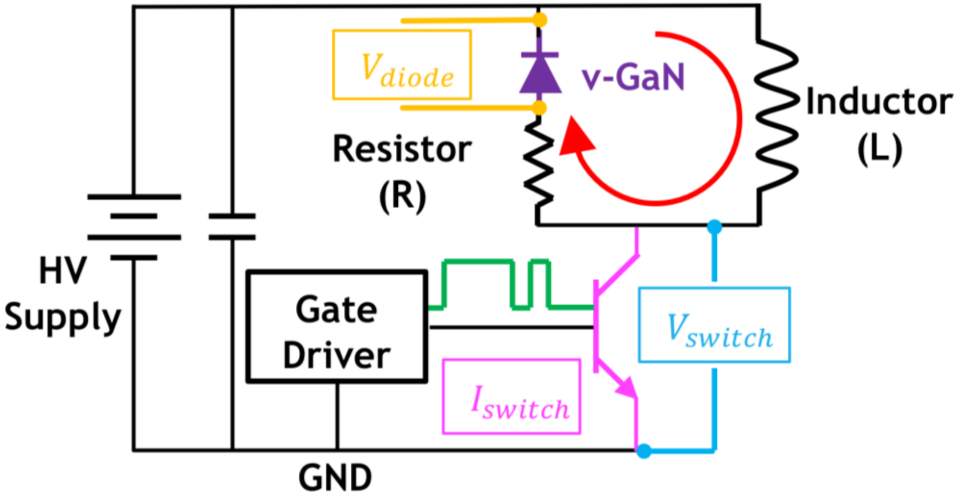


Leading ITRW materials and devices working group

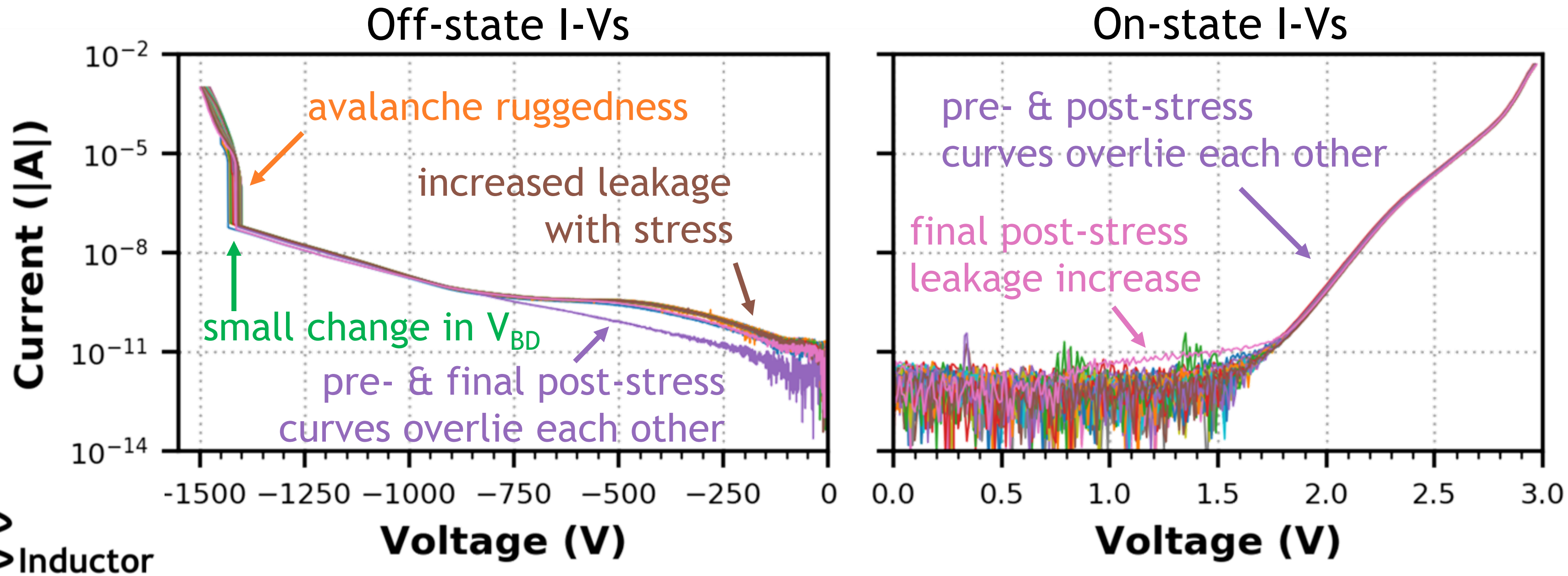
2020

Over 30 papers and presentations through the course of the project

Previous Results on GaN Diodes: Double-Pulse Testing



Cumulative v-GaN I-Vs over 720 minutes of 1000 V hard switching stress



- **The double pulse test circuit provides hard-switching stress, but does not transfer power**
- **This year's focus is to extend this work to a true power converter to better evaluate impact on real systems**
- **To this end, we have designed and fabricated a half-bridge converter to apply realistic stress profiles**

Beyond Double-Pulse Testing

Mission-Profile Based Reliability

- Device reliability depends on its *mission profile*, a complex set of application-specific operating parameters and environmental stressors
- Double-pulse testing provides simplified emulation of a mission profile – essentially only electrical stress
- For true representation of real-world performance, need to emulate practical operating conditions as accurately as possible

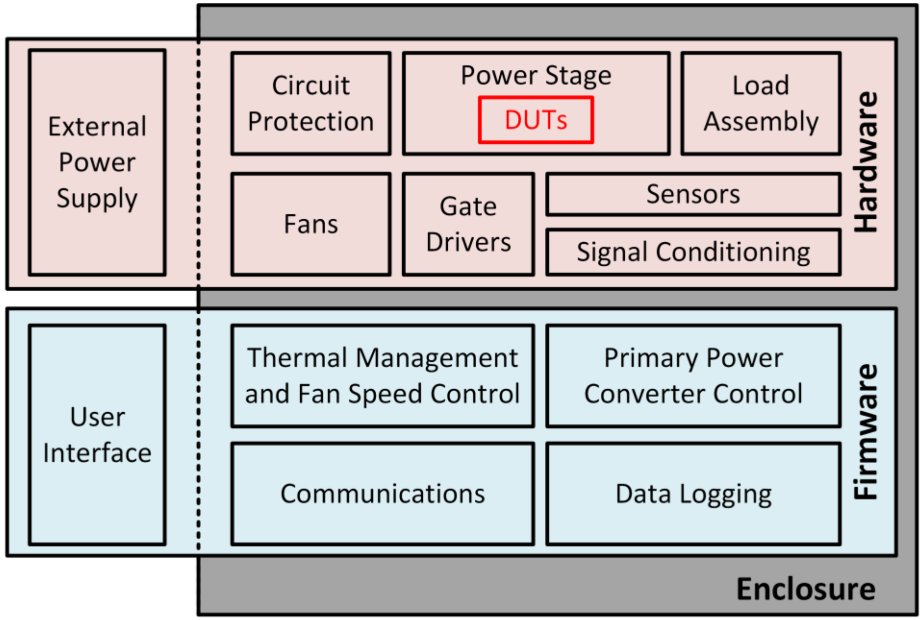
Value of Data from Practical Application Testing

- Represents a first step towards translating device-level characterization work to improvements in system-level performance
- Data are immediately useful for a variety of system integration tasks
  - Better tools for design and performance optimization
  - Improved estimates of remaining useful lifetime, more effective preventative maintenance scheduling
  - More effective methods of monitoring device and system integrity

Design of a Custom Component Assessment System (1)

Core Functions

- Emulate real-world conditions of a practical power converter deployment
- Apply user-specified stress patterns and mission profiles
- Record internal state variables and performance data during long-duration experiments
- Protect operators from electrical and kinetic hazards associated with practical converter failures

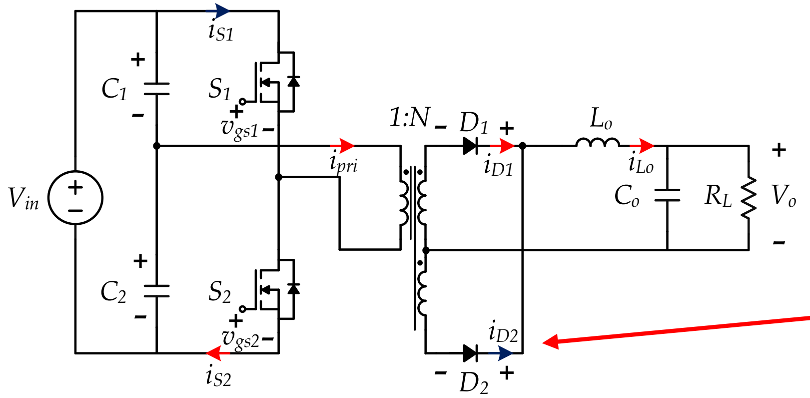


Dimensions:
16”×14”×8”

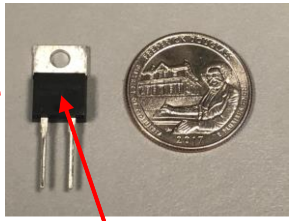
Design of a Custom Component Assessment System (2)

Power Stage

- Isolated half-bridge topology selected based on characteristics of v-GaN diodes
  - High forward voltage (~5 V)
  - High breakdown voltage (1200 V nominal)
- Half-bridge provides a balance between simplicity and flexibility



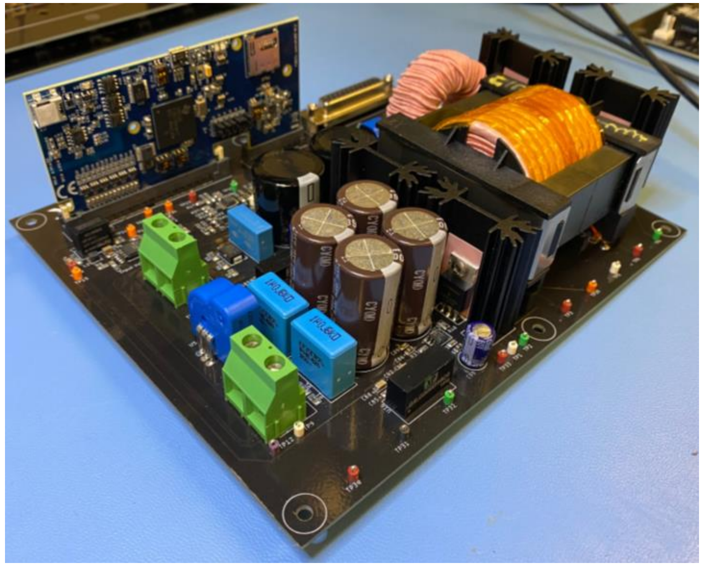
Packaged device under test



Device die

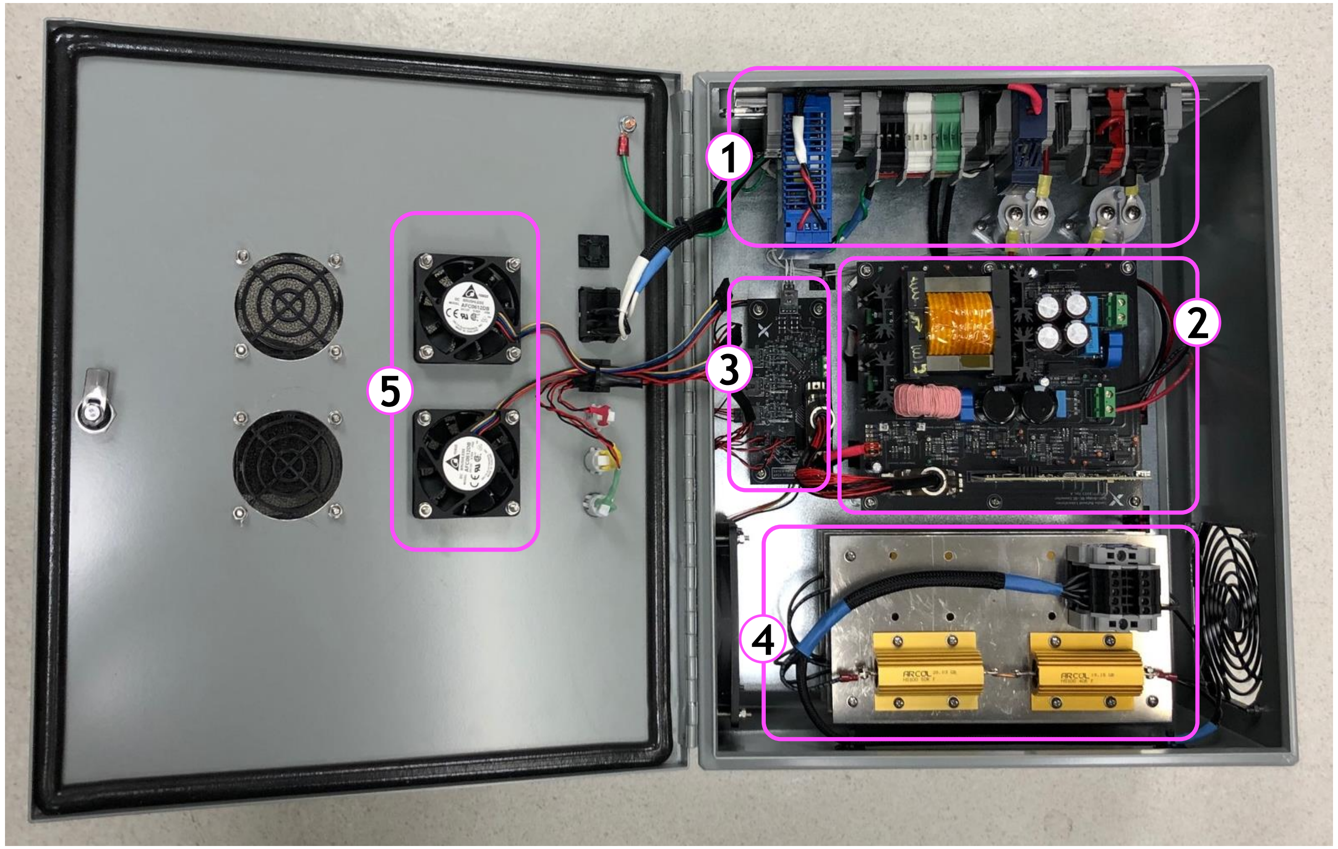
Experiment Control

- 32-bit DSP controls converter operation and maintains experiment parameters
- Diode parameters regulated:
  - Voltage stress (800 V < V_d < 1500 V)
  - Device junction temperature (ambient to 175˚C)
  - Forward current* (avg. 1 A nominal)
  - Switching frequency and duty cycle (100 kHz / 0.3 nominal)



* Current rating is limited by load assembly. Enclosure hardware will support up to 1500W load. Alternatively, the load may be replaced with a connection to external electronic load equipment.

Design of a Custom Component Assessment System (3)



1. Power entry, internal distribution, and circuit protection
2. Isolated half-bridge converter with on-board DSP control card
3. Enclosure control board
4. Configurable load assembly
5. PWM-controlled fans for DUT temperature control

Due to COVID lab access restrictions, spent considerable time designing the system for maximum flexibility and configurability

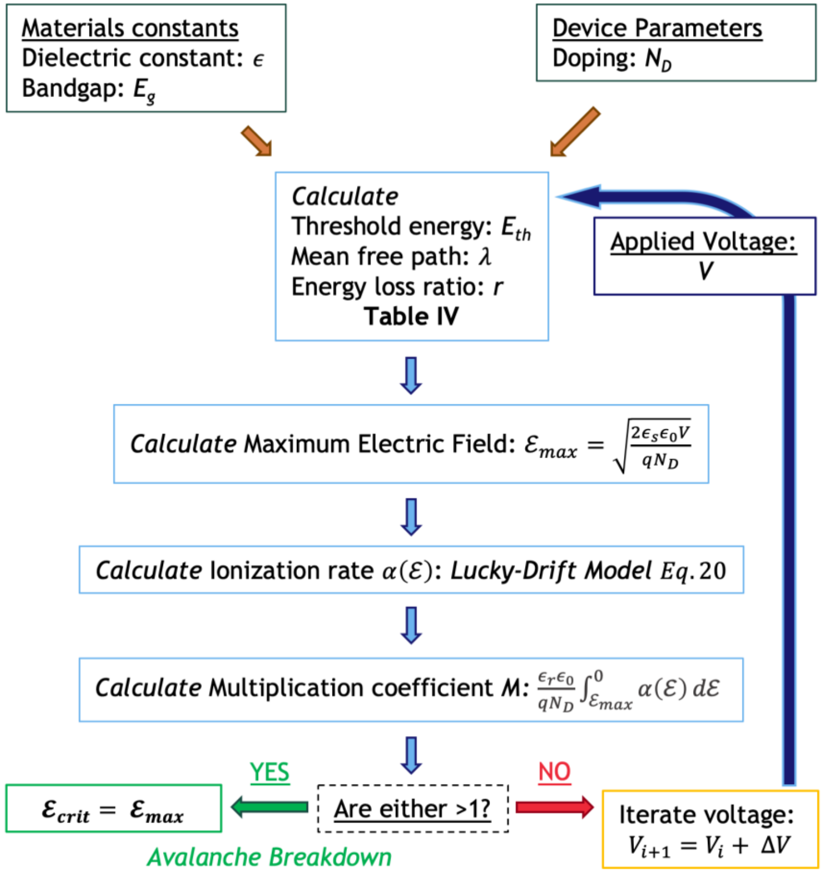
Towards Better Power Device Performance Projections

Critical Electric Field is an important parameter in design and use of power components

- Trade-off between switching loss and standoff voltage:

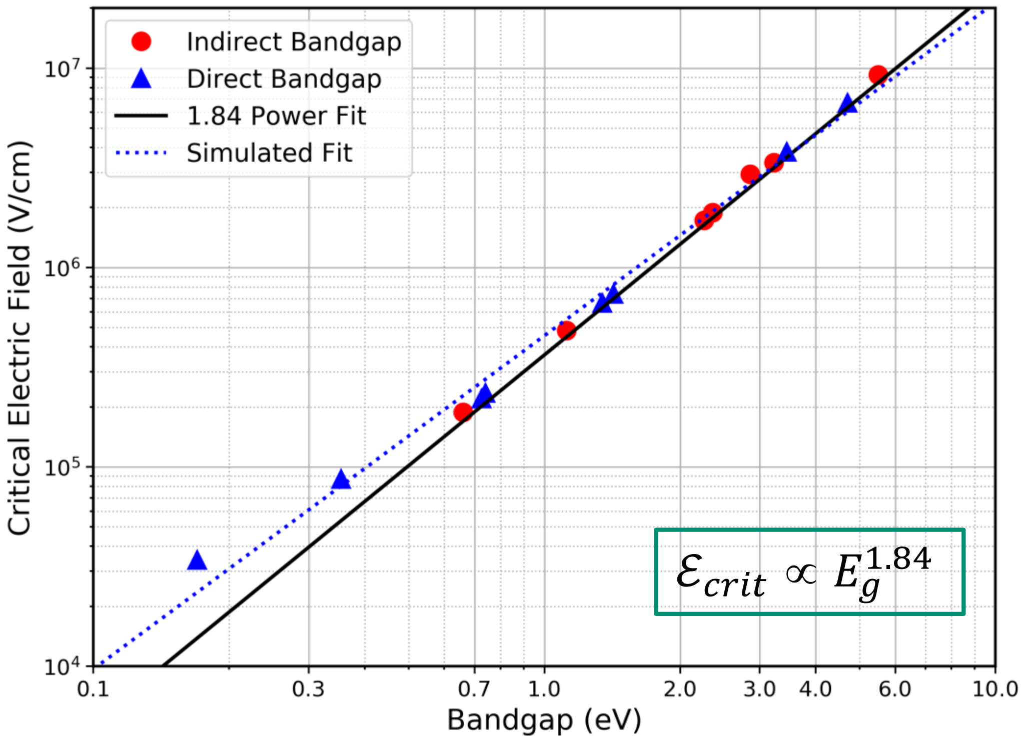
$\mathcal{E}_{crit} \propto E_g^{\gamma}$, $V_{BD} \propto \mathcal{E}_{crit}$ → $R_{ON,sp} \propto V_{BD}^2 E_g^{-3\gamma}$

First-order Model (Jack Flicker)



Old: $\mathcal{E}_{crit}$ (indirect-gap) $\propto E_g^{2}$, $\mathcal{E}_{crit}$ (direct-gap) $\propto E_g^{2.5}$

$R_{ON,sp} \propto V_{BD}^2 E_g^{-6}$ $\quad$ $R_{ON,sp} \propto V_{BD}^2 E_g^{-7.5}$

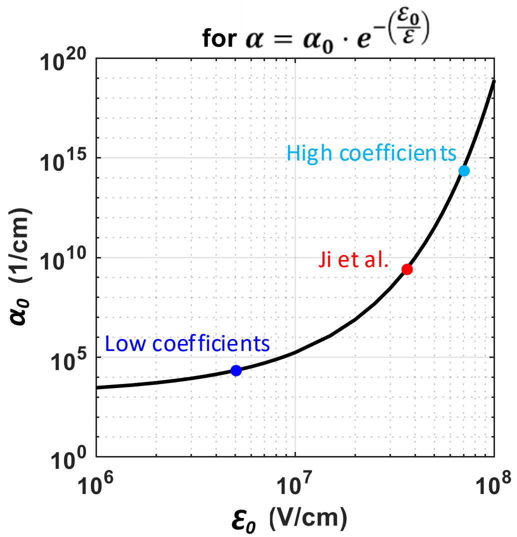


New: $R_{ON,sp} \propto V_{BD}^2 E_g^{-5.52}$

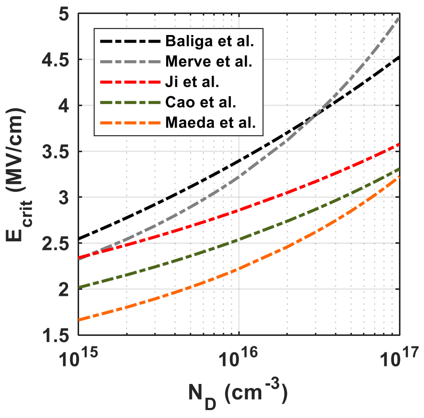
- Stronger performance dependence on bandgap

Limitations in Impact Ionization Modeling: 1D vs. 2D

Breakdown voltage depends only on E_{crit}, not on impact ionization parameters for ideal, 1D models

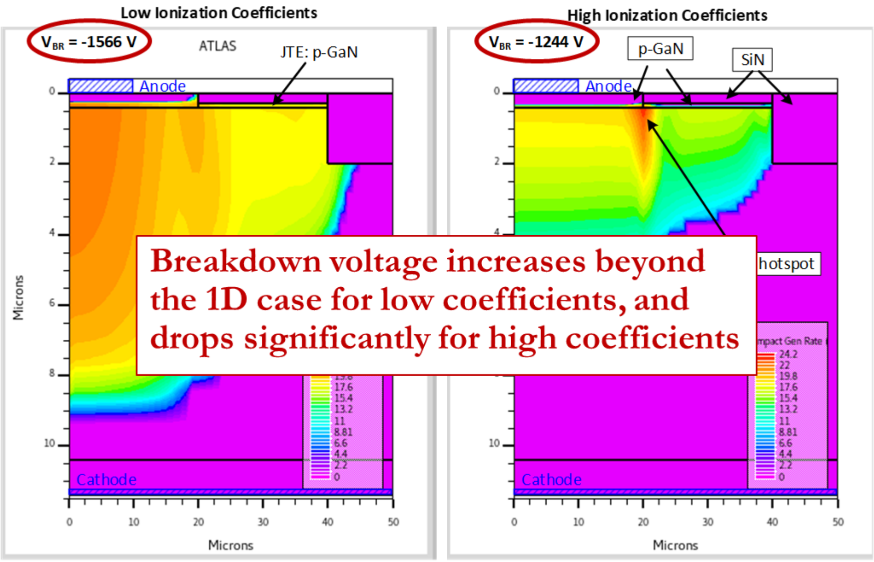


Significant variance in reported GaN impact ionization parameters leads to unreliable modeling



2D/3D models include non-idealities

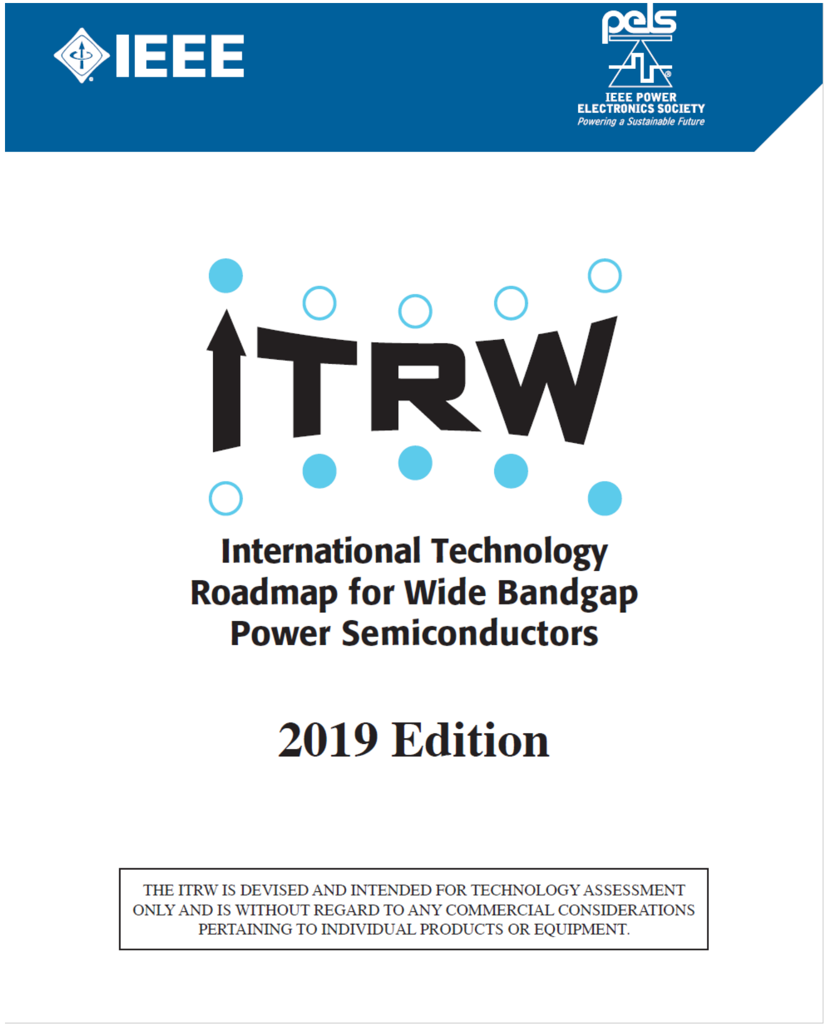
- Impact ionization parameters affect breakdown prediction



Two-Dimensional Model with Step-Etched JTE

A.T. Binder et al., *62nd Electronic Materials Conference, 2020.*

ITRW: Materials and Devices Group


IEEE

IEEE POWER ELECTRONICS SOCIETY
Powering a Sustainable Future

ITRW

International Technology Roadmap for Wide Bandgap Power Semiconductors

2019 Edition

THE ITRW IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

ITRW 1.0 → ITRW 2.0

Goal: to formulate a roadmap for wide-bandgap and ultra-wide-bandgap materials and devices

Primary topics:

1. SiC devices
2. GaN devices
   - HEMTs, integration, vertical GaN, etc.
3. UWBG materials

ITRW Special Issue: Open Journal of Power Electronics

- Call for papers – Sept 16th

IEEE-TV: ITRW Webinar

- Sept 16th – 9am and 2pm EDT

Publications

- V. Veliadis, R. Kaplar, J. Zhang, S. Khalil, J. Flicker, J. Neely, A. Binder, S. Atcitty, P. Moens, M. Bakowski, and M. Hollis, "International Technology Roadmap for Wide-Bandgap Power Semiconductors Chapter 6: Roadmap for WBG and UWBG Materials and Devices," IEEE, 2019 Edition. Also presented at the ITRW Kick-Off Meeting at the IEEE Energy Conversion Congress and Exposition, Baltimore, MD (September 2019).
- A. T. Binder, R. J. Kaplar, and J. R. Dickerson, "Limitations in Impact Ionization Modeling for Predicting Breakdown in Wide Bandgap Power Semiconductors," 2020 Virtual Electronic Materials Conference (June 2020).
- O. Slobodyan, J. Flicker, J. Dickerson, A. Binder, T. Smith, R. Kaplar, and M. Hollis, "Analysis of the Dependence of Critical Electric Field on Semiconductor Bandgap," submitted to *Journal of Applied Physics* (August 2020).

Questions?

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Stan Atcitty: satcitt@sandia.gov

We thank the DOE Office of Electricity Energy Storage Program managed by Dr. Imre Gyuk for supporting the work at Sandia National Laboratories